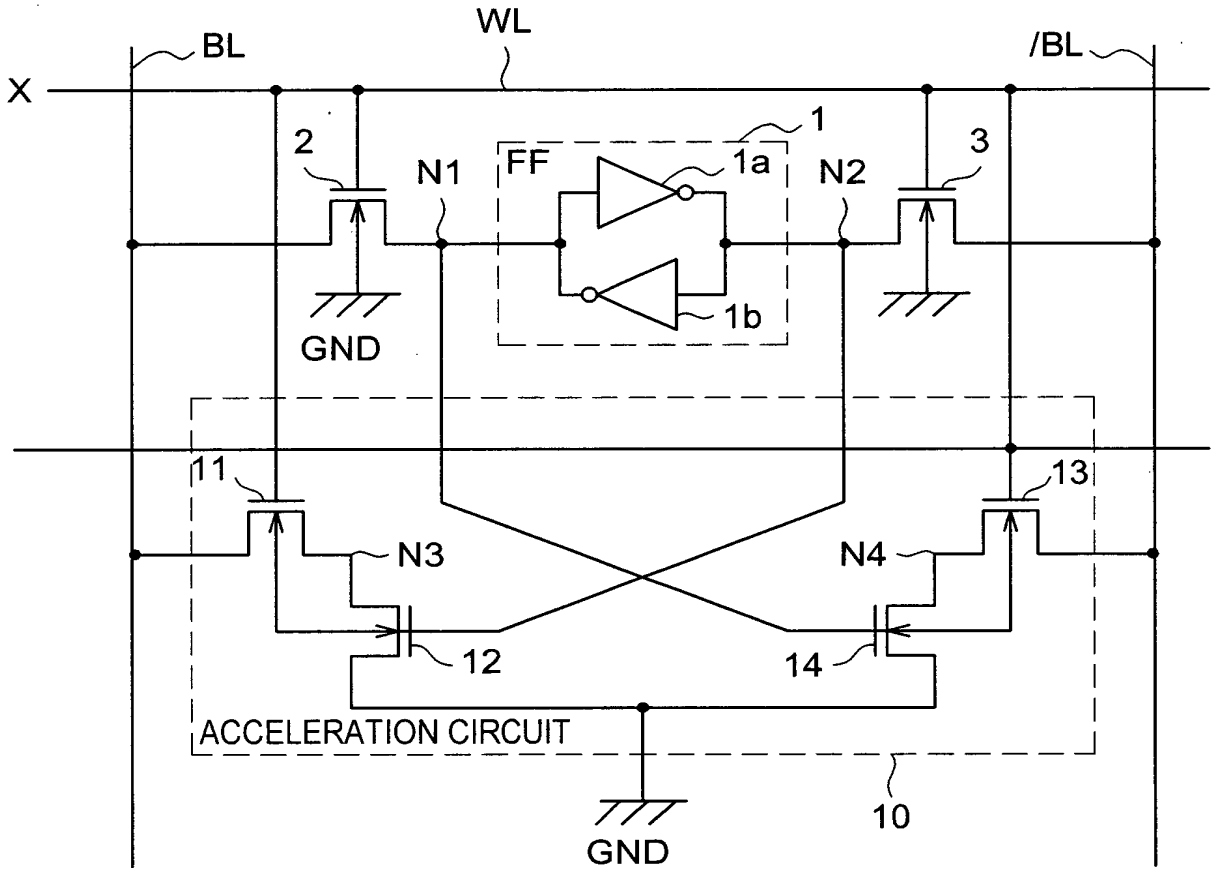
FIG.1


WL
BL
/BL
X
2
N1
FF
1
1a
1b
N2
3
GND
11
13
N3
N4
12
14
ACCELERATION CIRCUIT
10
GND

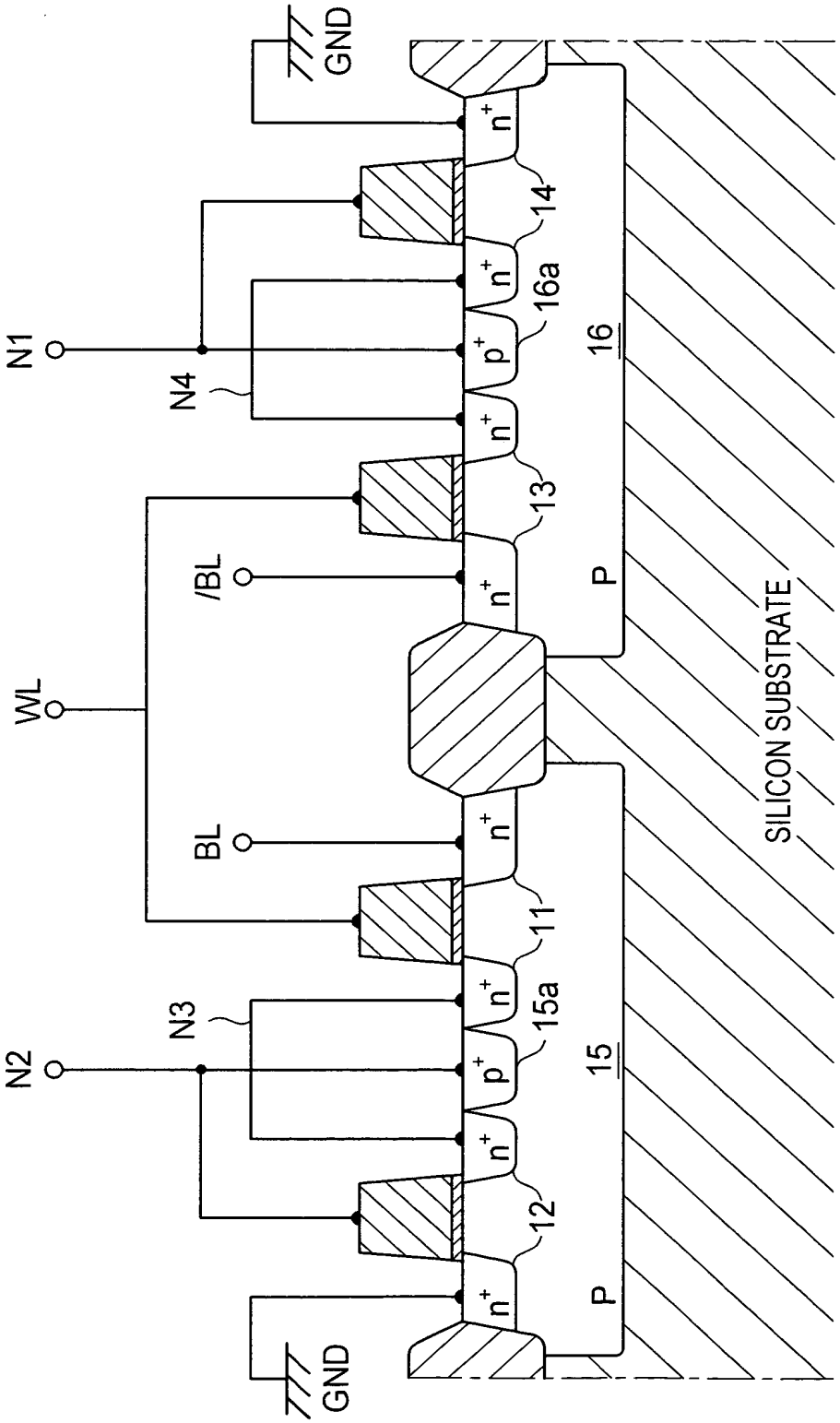

GND
N1
N4
WL
/BL
BL
N2
N3
GND
n+
p+
14
16a
16
13
11
15a
15
12
P
P
SILICON SUBSTRATE

FIG.2

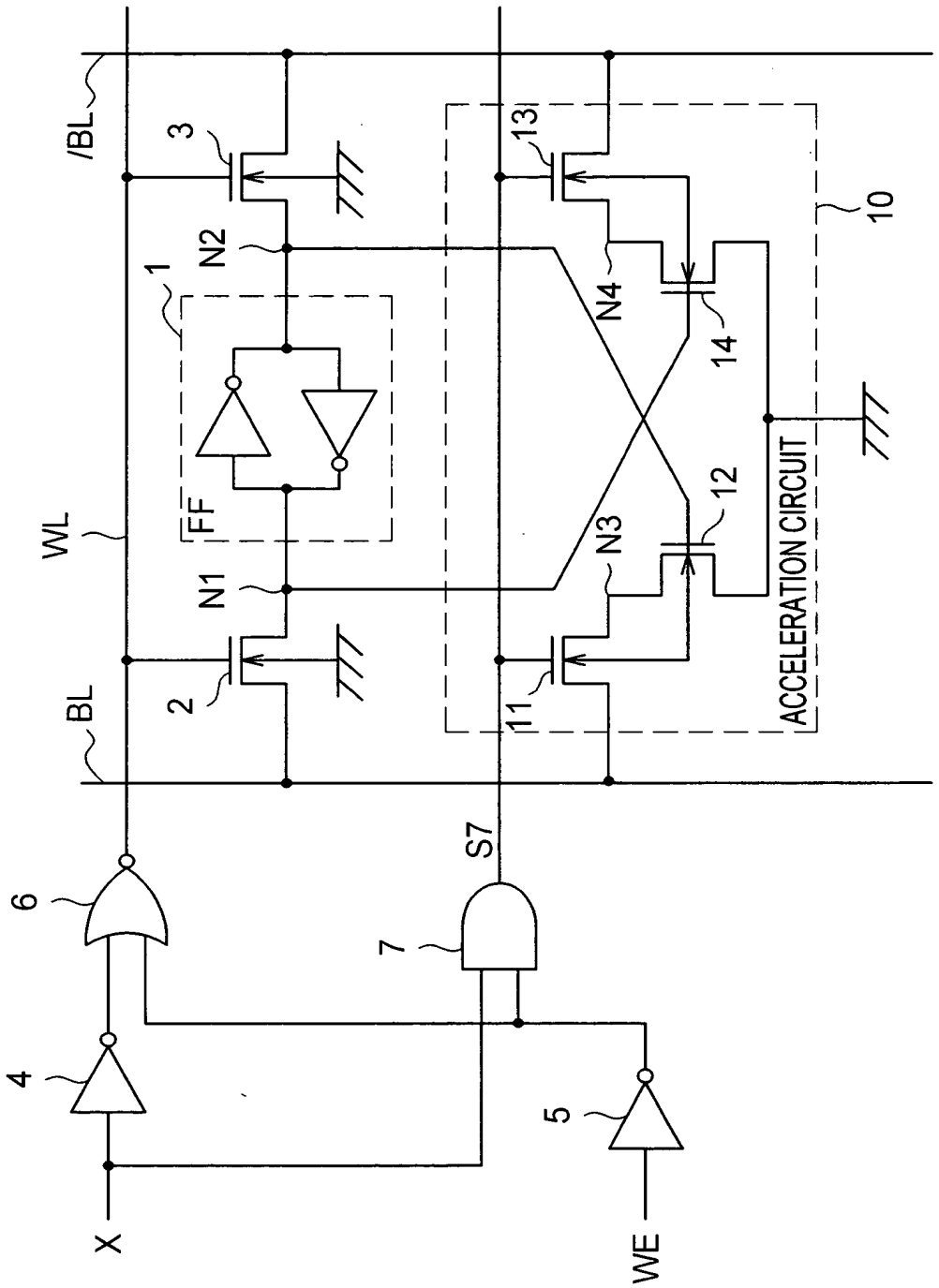

/BL
BL
WL
FF
N1
N2
N3
N4
1
2
3
4
5
6
7
10
11
12
13
14
S7
X
WE
ACCELERATION CIRCUIT

FIG.3

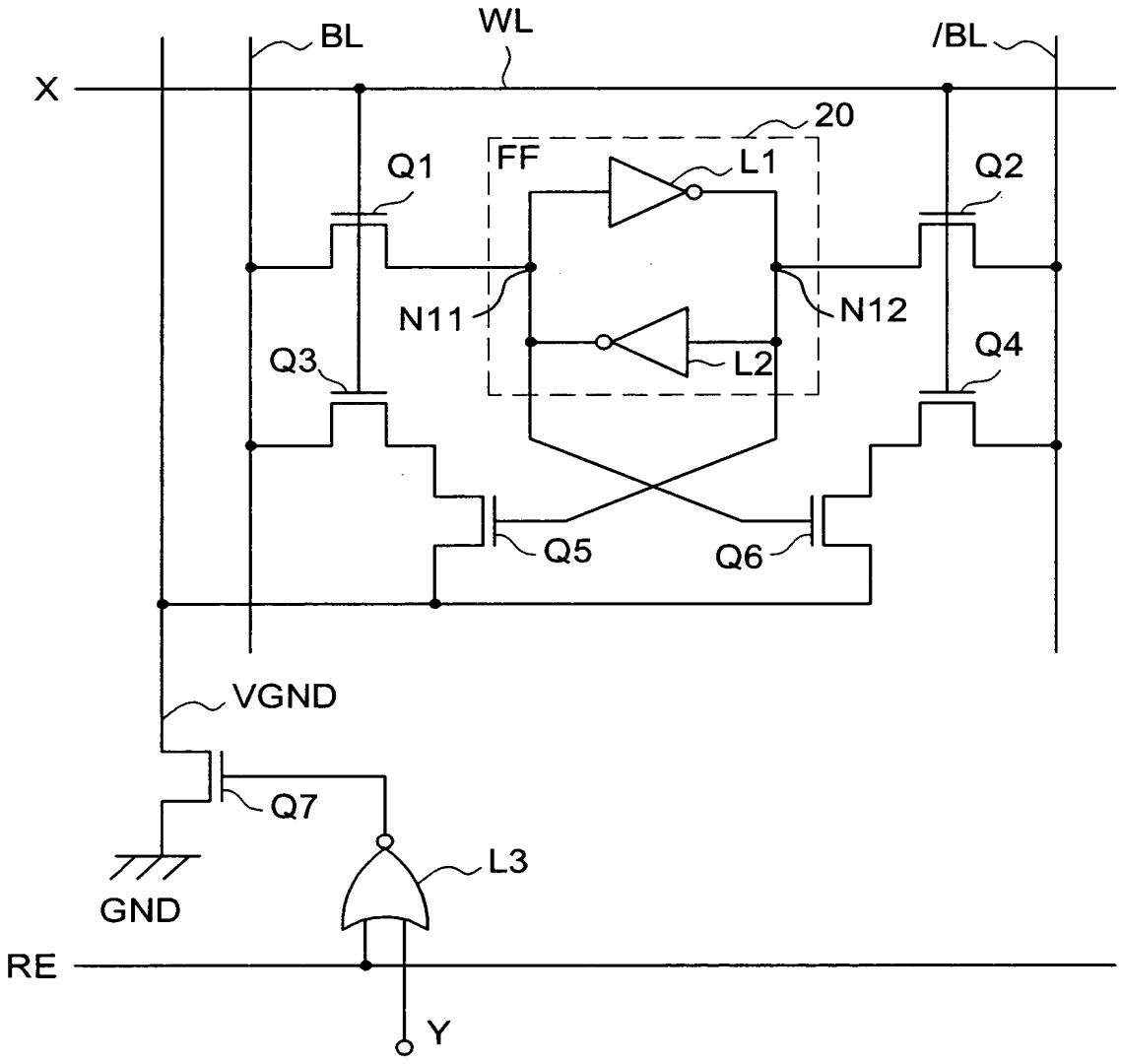



FIG.4